Phase Locked loop Operable Over a Wide Frequency Range

Related Application:

This application is a non-provisional application of provisional application serial

5 number 60/458,085 filed 3/26/03. Priority of application 60/458,085 is hereby

claimed.

Field of the Invention:

The present invention relates to electronic circuits and more particularly to

10 electronic phase locked loops.

Background of the invention:

Phase-locked loops (PLLs) are feedback control systems that are often an

essential part of many telecommunications devices. PLLs are used in

15 modulators and demodulators, in frequency synthesizers, in clock

synchronizations circuits and in many other high-speed communication

applications. PLL can be implemented using digital or analog devices.

Figure 1 shows a block diagram of a conventional PLL. The PLL shown in Figure

20 1 includes four main components, namely, a Phase Frequency Detector (PFD)

11, a Filter 12, a Variable Frequency Oscillator (VFO) 13 and feedback loop with

a frequency divider 14. The VFO 13 could for example be a Voltage Controlled

Oscillator (VCO).

The PFD 11 compares the phase and frequency of the feedback signal to the reference signal and it generates an error signal indicating any difference it detects. The error signal generated by PFD 11 passes through the filter 12 and is used to adjust the frequency of the VFO 13. Any differences between the input

5 signal and the feedback signal are thus used to change the frequency of the VFO.

A PLL can be used as a frequency multiplier. For example, in the circuit shown in Figure 1, the output of the reference signal may be a 10 Mhz signal. The output

10 of the VCO may for example be a 1Ghz signal. In such a PLL the frequency divider 14 would divide the 1 Ghz output signal down to a 10Mhz signal. The frequency divider 14 can be adjusted to a higher or lower divisor in order to change the output frequency of the PLL.

15 There is great deal of published literature which describes the design and operation of prior art PLLs. For example, PLL technology is described in a text book entitled "Phase-Locked Loops" by Roland Best, ISBN: 0071412018, dated June 20, 2003. Other books and literature which describe the principles and applications of PLL are also available.

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An important parameter which affects the operation of a PLL is the loop "gain". An important component of loop gain is the gain of the VFO. Gain of a VFO is a measure of the change in the output of the VFO relative to changes in the input signal to the VFO. Where the VFO is a Voltage Controlled Oscillator (a VCO),

the gain of the VCO (or of the PLL) is often expressed as mega-hertz per volt (MHz/V). Generally, for a particular PLL, it is desirable to have a constant loop gain over the entire range of frequencies at which the PLL operates. If the loop gain differs at different frequencies, the lock time, the bandwidth, and other

5   parameters of the PLL may change when the operating frequency changes and this may adversely affect the PLL.

In some applications, a PLL must be able to operate over a wide frequency range. In many such applications it is desirable to have a loop gain that does not

10   significantly change as the operating frequency changes even though the frequency changes cover a wide range. The present invention is designed to provide an improved PLL which has substantially constant loop gain over a wide frequency range.

15   **Summary of the Invention:**

With the present invention the frequency range over which the PLL operates is divided into a number of frequency sub-ranges. A mechanism is provided for adjusting the loop gain profile as the PLL moves from one frequency sub-range to another. When the PLL switches to a new frequency sub-range, the loop gain

20   profile is adjusted to a pre-established value. Changes in frequency within each sub-range are then accomplished with the loop operating within a specified range of gain. In one preferred embodiment, the VFO is a VCO and the loop gain profile is adjusted by adjusting the gain profile of the VCO.

Brief Description of the Figures:

Figure 1 is a block diagram of a prior art Phase Locked Loop.

Figure 2 is a block diagram of first embodiment of the invention.

Figure 3 is a diagram showing VCO gain at various settings.

5 Figure 4 is a circuit diagram of a VCO with variable gain.

Figures 5A and 5B are block diagrams illustrating the operation of the system.

Figure 6 is a block diagram of an alternate embodiment of the invention.

Description of Embodiments:

10 A block diagram of a first preferred embodiment of the invention is shown in

Figure 2. This embodiment includes a reference signal 200, a Phase Frequency

Detector (PFD) 201, a filter 202, a Voltage Controlled Oscillator (VCO) 203, a

feedback loop that includes a frequency divider 204 and control logic 210 and

211. A VCO is a type of Variable Frequency Oscillator (VFO). The frequency of

15 the VCO 203 is controlled by the output signal from filter 202. Additional detail

concerning VCO 203 are given below with reference to Figure 3 and the

operations performed by logic 210 and 211 are described below with reference to

Figures 5A and 5B. The PFD 201 and the filter 202 can be state of the art

components.

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The PLL shown in Figure 2 is a feedback control system that automatically

adjusts the phase and frequency of the signal generated by VCO 203 (after it is

divided by divider 204) to match the phase and frequency of reference signal

200. When in a locked condition, any slight difference between the reference

signal 200 and the VCO output (as divided by divider 204) appears as a phase difference. This phase difference causes PFD 201 to generate an error signal. The error signal is first is smoothed by filter 202 and it then acts to change the frequency of VCO 203. Stated differently, the PFD 201 generates a signal that

5   adjusts the control voltage presented to the VCO 203 until the feedback frequency matches that of the reference signal. When the system is phase-locked, the frequency of the output of VCO 203 is N times that of the frequency of reference signal 200. (where N is the division performed by divider 204). Changing the value of the divider 204 will cause the PFD 201 to sense a

10   frequency or phase error. The PFD 201 will then generate an error signal which will change the frequency of VCO 203.

The PLL shown in Figure 2 is a nonlinear device because the phase detector 201 is of necessity non-linear(as is the case with most PLLs). However, when the

15   loop is in a locked condition, the PLL can be approximated by a linear model. In this case, each of the PLLs components can be described by linear transfer function and various types of gain can be defined. For example one can define, the forward gain, the open loop gain and the closed loop gain. In general, the closed-loop gain is equal to the forward gain divided by (1 + the open loop gain).

20   The definition of gain must take into account both phase and frequency. The open loop gain, the forward gain, and the closed loop gain are all related. Thus changing either the forward gain, the open loop gain or the closed loop gain is a change in the other gains. The values of the specific elements which form the loop must be chosen so as to satisfy the normal stability requirements. The filter

202 can be a first, second, third, etc order filter as the requirements of a particular application may require.

The various gain parameters which define the PLL are determined by the characteristics of all of the components in the in the loop. That is, for example, the loop gain of the PLL shown in Figure 2 is determined by combined the characteristics of PFD 201, filter 202, VCO 203, and frequency divider 204. However, the gain provided by the VCO is a major factor in a PLL's loop gain.

The forward gain, the open loop gain and the closed loop gain of the PLL shown in Figure 2 is a function of the frequency at which the PLL is operating. That is, gain changes as a function of frequency. Herein the term "gain profile" is used to describe the way in which the gain of the PLL changes relative to frequency. The gain and the gain profile of a PLL Techniques can be experimentally and analytically determining.

Changes in a variety of the components in a PLL can change the gain profile of the PLL. In the specific embodiment described herein, the gain profile of the loop is changed by changing the value of certain components in the VCO 203. It should be understood that in other embodiments, the gain profile of the loop can be changed by changing components in other units that form part of the PLL loop.

The gain of a VCO is often expressed as mega-hertz per volt (MHz/V).

The gain of VCO 203 is a measure of the change in the output of the VCO relative to changes in the input signal from the filter 202. The gain profile of a VCO defines how gain varies as frequency changes. Figure 3 shows the gain of the VCO 203 plotted against the frequency. Three gain profiles, termed "Gain

5   Curve A", "Gain Curve B, and "Gain Curve C" are shown in Figure 3. The particular shape of the gain profile for VCO 203 depends upon the value of the components in the VCO. As will be explained in detail later, with the present embodiment, the value of certain components in the VCO 203 can be changed. Thus, the three gain profiles shown in Figure 3 represent the operation of VCO

10   203 when certain components in the VCO are set to three different values.

With the present embodiment of the invention, the gain profile of the VCO 203 can be changed by an external signal. That is, the value of certain components in VCO 203 can be controlled by an external signal. As will be explained with

15   reference to Figure 3, the gain profile of VCO 203 is controlled by signals from gain profile control logic 210.

Figure 3 shows three different gain curves that represent the gain of VCO 203 at three different settings provided by gain profile control logic 210. Each gain curve

20   illustrates a different gain profile for the VCO 203.

As illustrated in Figure 3, at each gain profile setting, the gain varies over the frequency range. In this particular preferred embodiment, the operating frequency range is divided into three different frequency sub-ranges designated

frequency sub-ranges A, B and C. Naturally, the number of frequency sub-ranges selected is an engineering choice for each particular application. At each gain profile setting, the VCO gain varies over frequency as indicated by gain curves A, B and C. With the particular embodiment shown here, in order to

5   satisfy the other requirements of the system, it is desirable to maintain the VCO gain between the values indicated as x and y in Figure 3. The particular values established as acceptable gain are a matter of engineering choice for each particular application of the PLL.

10   For example in one particular embodiment the curves shown in Figure 3 have the following values:

frequency sub-range A: between 2.4 and 2.43 GHz,

frequency sub-range B between 2.43 and 2.45 GHz

frequency sub range C between 2.45 and 2.48 GHz.

15   acceptable gain low value x: 0.26 GHz/V

acceptable gain high value y: 0.325 GHz/V.

The gain profile of the VCO 203 can be controlled by a signal from the Gain Profile Control Logic 210. The details of how the Gain Profile Control Logic 210

20   controls the gain profile of VCO 203 is described later with respect to Figure 4.

With the present invention the gain is maintained between the x and y values across the entire frequency range of operation by changing the gain profile of the VCO 203 so that the VCO 203 operates on gain curve A in frequency sub-range

A, on gain curve B in frequency sub-range B, and on gain curve C in frequency sub-range C.

It is noted that considering the overall system operation, (that is, the combination of sub-range A, sub-range B and sub-range C) the gain is relatively symmetrical about the center frequency of the entire range. As used herein the term center frequency refers to the center frequency of the entire range of frequencies at the output of the VCO.

Figure 4 is a circuit diagram of VCO 203. VCO 203 one specific type of VFO. The difference between VCO 203 shown in Figure 4 and a normal VCO, is that the gain profile of the VCO shown in Figure 4 can be changed by an external signal. The VCO shown in Figure 4 includes a bi-stable circuit, one side of which has a coil 410, a capacitor 411 and a transistor switch 414 and the other side of which has a coil 412, a capacitor 413 and a transistor 415. The circuit has a bias control transistor 416. The frequency of the circuit is controlled by a control signal applied at frequency control point 430. Such a bi-stable circuit is can be designed and implemented using state of the art technology.

The circuit shown in Figure 4 also has gain profile control circuits 450 and 460. It is circuits 450 and 460 that differentiate the VCO shown in Figure 4 from other VCO circuits. Circuits 450 and 460 are identical and they are operated in a synchronized fashion, hence, only circuit 450 will be explained in detail. Circuit 450 has a variable capacitor 451. A signal from the Gain Profile Logic 210

(shown in Figure 3) controls the value of capacitor 451. Changing the value of capacitors 451 and 461 changes the gain profile of the VCO. That is, changing the value of capacitors 451 and 461 changes the shape and position of the curve which shows how gain changes with frequency. There are various ways of

5   changing the values of capacitors such as capacitors 451 and 461 and the particular manner that the capacitance values are changed is not significant to the embodiment. The signals from Gain Profile Control 210 could be analog or digital control signals which change the value of capacitors 451 and 461.

10   The specific values of the coils, capacitors and other elements of the circuit shown in Figure 4 are not relevant to the present invention. The present invention is directed to the overall system configuration and not to the details of the VCO. The VCO shown in figure 4 is merely a specific example of a VCO the gain profile of which can be controlled. There are numerous other ways that the

15   gain profile of a VCO could be controlled. The embodiment shown merely requires a VCO, the gain profile of which can be controlled. As explained below, other embodiments of the invention utilize other types of Variable Frequency Oscillators (VFOs) the gain profile of which can be controlled by an external signal.

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The overall operation of the system shown in Figure 2 is shown by the block diagrams given in Figures 5A and 5B. Figure 5A shows how the appropriate values for capacitor 451 and 461 are determined for the various frequency sub-ranges. As indicated by block 501, the frequency response of the VCO is

measured at various settings of capacitor 451 and 461. This in effect generates a series of curves such as those shown in Figure 3. For each desired frequency sub-range, the value of the capacitors 451 and 461 which produces a gain curve with values within the desired boundaries is determined and stored as indicated by block 502. It is noted that the gain can also be determined by various other analytical techniques. Various methods and techniques can be used to determine the gain of a VCO.

The logical operations performed by Gain Profile Control Logic 210 and Frequency Control and Decision Logic 211 and the normal operation of the system is illustrated in Figure 5B. The operations illustrated in Figure 5B occur after the values determined by the process illustrated in Figure 5A have been stored in Gain Profile Control Logic 210. The process begins at block 510 when the system receives a command to set the output of the system to a new frequency value. As indicated by block 511, the sub-range into which the new frequency falls is determined. The appropriate value for divider 204 is determined in a normal manner. The appropriate value for capacitors 451 and 461 for this particular sub-range are then retrieved from where they were stored as indicated by block 512. The capacitors are then set to this new value and the divider 204 is set to the appropriate value. Alternatively, the sequence can be reversed, that is, the divider can be first adjusted and then the capacitors can be reset. In still another alternative embodiment, both changes can be made simultaneously. The above operations are performed by Gain Profile and Control Logic 210 and Frequency Control and Decision Logic 211. Such logic is can be

performed by a set of discrete logical components or it can be performed by a programmed microprocessor. The division of the logic into two units 210 and 211 is solely for the purpose of ease of explanation and all the logic could be in one unit.

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Various other embodiments of the invention are possible. For example alternate embodiments of the invention can use other types of Variable Frequency Oscillators (VFOs), the gain profile of which can be varied by an external signal. One alternate embodiment utilizes a VFO, the frequency of which is controlled by

10   a current signal instead of by a voltage signal.

The oscillator shown in Figures 2 and 4 is a VFO the frequency of which is controlled by voltage signal 430 and the gain profile of which is controlled by an external signal from logic 210. Alternate embodiments of the invention can

15   include a VFO, the frequency of which can be controlled by a current signal (or by a digital signal) and the gain profile of which can be controlled by an external signal. Various components can be changed by an external signal so as to change the gain profile of the VFO. Variable Frequency Oscillators the frequency of which is controlled by a voltage signal, a current signals, or a digital signals

20   can be used in various embodiment of the invention.

The term variable frequency oscillator (VFO) is meant to include oscillators, the frequency of which can be controlled by a voltage signal, a current signal or by a digital signal. With respect to Figure 4, in alternate embodiments, the control

signal 430 could be a current signal or a digital signal. To implement the present invention, what is needed is a VFO, the gain profile of which can be controlled by an external signal. That is, one of its parameters must be controllable by an external signal so that its gain profile can be controlled. Alternate embodiments of the invention use other types of VFOs, the gain profile of which can be varied by an external signal. The VCO shown in Figure 4 is merely meant as an example of a VFO the gain profile of which can be controlled by an external signal.

Figure 6 shows still another alternate embodiment of the invention. The difference between the embodiment shown in Figure 2 and the embodiment shown in Figure 6, is that in the embodiment shown in Figure 6, the reference signal 200, goes through a frequency divider 260 , before the signal goes to the PFD 202. This gives the system a wider frequency range. In the embodiment shown in Figure 6, the control logic 211 not only controls the division 204 and the gain control 210, but it also controls divider 260 which divides reference signal 200. Whether or not divider 260 is necessary to obtain the desired frequency range is a matter of engineering design. Use of such a frequency divider for the reference signal can increase the frequency range of the system.

In still another alternative embodiment (not shown in the Figures), control 211 merely controls divider 260 and gain control 210. In such an embodiment, the control of divider 204 could be by an entirely independent control, or divider 204 could be set at a fixed divisor.

The systems shown in Figures 2 and 6 could be built on a single integrated circuit chip. Alternatively, various components can be located on different chips. How the components are assigned to specific chips is a matter of engineering design.

5   The system can be implemented as an analog (i.e. linear) circuit or as a digital circuit. Alternatively the system can be implemented as a hybrid circuit with some analog and some digital components. The logic circuits 210 and 211 can be implemented as special purpose logic or they could be implemented using microprocessor control logic. In still another alternative embodiment, the entire

10   system could be implemented using a programmed computer and a computer program which simulates the various components in the system.

It is noted that the particular filter chosen for a particular PLL depends upon the specific application of the PLL. For example, filter 202 could be a charge pump.

15   The order of filter 202 is not relevant to the present invention and it is a matter of engineering design. The PFD 201 and the filter 202 can be designed and implemented as required by the particular applications for which a particular embodiment is designed.

20   It is noted that the system could be implemented as an integer N frequency synthesizer which creates a set of frequencies that are an integer multiple of a fixed reference frequency. Alternatively, the system could be implemented as a fractional N frequency synthesizer which produces frequencies that are an Nf (N times F) multiple of a fixed reference (where N is an integer and f is a fractional

part of an arbitrary number. Such embodiments involve various relationships between the divider 204 and any divider of reference signal 200.

In the preferred embodiment shown in detail herein the loop gain profile is varied

5   by varying the gain profile of the VFO. In still other alternate embodiments, the loop gain of the PLL is varied by changing components in elements of the PLL other than the VFO.

While the invention has been shown and described with respect to a number of

10   embodiments thereof, it should be understood that various other changes in form and detail may be made without departing from the sprit and scope of the invention.

I claim:

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